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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,780	07/24/2001	Taketoshi Nakano	70840-56281	3887

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,780	NAKANO ET AL.	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8/16/04* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-8 are presented for examination.

2. The after final Amendment filed on 8/16/2004 is entered.

3. The rejection of claims 1-4 is withdrawn but the rejection of claims 5-8 is maintained.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent # 6,025,822 ("Motegi et al.).

As for claim 5, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits arranged in a line and provided along a first side of the display panel; and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits arranged in a line and provided along a second side of the display panel, the second side being adjacent to the first side, wherein: controller Fig.1 (2) a control data signal for driving the display

panel is input to a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, a level shifter circuit Fig.1 (14b) includes a timer corresponding to a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits is generated in the first column electrode driving circuit, and the generated timing signal and a data signal are output to a second column electrode driving circuit, among the plurality of column electrode driving circuits, which is directly connected to the first column electrode driving circuit, the output data signal is transferred to a third column electrode driving circuit, among the plurality of column electrode driving circuits, which is directly connected to the second column electrode driving circuit, and the generated timing signal is transferred in a cascading manner to the plurality of row electrode driving circuits as a scanning signal.

As for claim 6, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits connected in series arranged in a line on a printed circuit board provided along a first side of the display panel (it is inherent for the semiconductor integrated circuit to include a printed circuit board); and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits connected in series arranged in a line and provided along a second side of the display panel, the second side being adjacent to the first side, wherein: a controller Fig.1 (2) includes all of the circuits before going to the display panel (TCP)

corresponding to each of the plurality of column electrode driving circuits is mounted in a tape carrier package, a first column electrode driving circuit, among the plurality of column electrode driving circuits, which is closest to the plurality of row electrode driving circuits, generates a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and controller Fig.6 (2) includes all the components before outputting to display panel (TCP) corresponding to the plurality of row electrode driving circuits, and outputs the generated timing signal to a first row electrode driving circuit, among the plurality of row electrode driving circuits, which is closest to the first column electrode driving circuit as a scanning signal, a timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially through a first line portion provided on the tape carrier package mounting the first column electrode driving circuit, a second line portion provided on the printed circuit board, a third line portion provided on the tape carrier package mounting the first column electrode driving circuit, and a fourth line portion provided on the display panel.

As for claim 7, Motegi et al. teach a display panel Fig.7 (20); semiconductor integrated circuit column drivers Fig.7 (21) corresponding to a plurality of column electrode driving circuits connected in series arranged in a line on a printed circuit board provided along a first side of the display panel (it is inherent for the semiconductor integrated circuit to include a printed circuit board); and row drivers formed a semiconductor integrated circuit Fig.7 (22) corresponding to a plurality of row electrode driving circuits connected in series arranged in a line and provided along a second side

of the display panel, the second side being adjacent to the first side, a controller Fig.7 (23) is to write input display data in a RAM 24 once and to supply control signals to the column drivers 21 and row drivers 22 through control signal lines 25, 26 (column 1, lines 51-53) corresponding to a timing signal for controlling the plurality of row electrode driving circuits is supplied to one of the plurality of row electrode driving circuits sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel.

As for claim 8, Motegi et al. teach a liquid crystal panel Fig.7 (20); a plurality of column electrodes provided along a first side of the of the display panel Fig.7 (21); a plurality of row electrodes provided along the second side of the display panel adjacent to the first side Fig.7 (22), a controller 23 connected to the first column driver 21 which is connected in series with all the of the column drivers and connected to the row drivers 22 where the controller provides to the column and row drivers with a signal circuit and a timing circuit inherently. Accordingly, the prior art does not teach explicitly that a first column electrode driving circuit generates a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits and outputs the generated timing signal to a first row electrode driving circuit, among the plurality of row electrode driving circuit, which is closest to the first column electrode driving circuit as a scanning signal. However, the prior art teaches a controller fig.7 (23) connected to the column drivers (21) connected in series with each other and row electrode drivers (22) corrected in series with each other where said

controller provides the row and column drivers with a signal circuit and a timing signal inherently.

Thus, it would have been obvious to a person of ordinary skill in the art to a first column electrode driving circuit generates a timing signal for controlling an operation timing to achieve the teaching of the prior art using the controller, the column electrode drivers, and row electrode drivers because this would provide a column electrode driving semiconductor integrated circuit and a row electrode driving semiconductor integrated circuit which can reduce the number of elements such as a memory in a liquid crystal driving circuit, and realizes the reduction of a power consumption rate by lowering the speed of processing. It is also well know in the art to combine two integrated circuits.

Allowable Subject Matter

5. Claims 1-4 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the claimed invention is directed to a plurality of column driving circuits and row driving circuits in a matrix type display device. Independent claim 1 identifies a uniquely distinct feature " a data input section Fig. 4A (13a) for receiving a control data signal for the plurality of column electrodes; a timing control section Fig.4A (13) for generating a timing control signal for controlling at least one of the row electrode driving circuit and the column electrode driving circuit; a selection section (13c) for selecting one of a signal in synchronization with the timing signal generated by the timing control section

and the control data signal input to the data input section, based on the control data signal input to the data input section; a data output section (13d) for outputting one of the signal in synchronization with the timing signal and the control data signal which is selected by the selection section, wherein the data input section of a second column electrode driving circuit of the plurality of column electrode driving circuits is connected to the data output section of a first column electrode driving circuit of the plurality of column electrode driving circuits, and the data output section of the second column electrode driving circuit is connected to the data input section of a third column electrode driving circuit of the plurality of column electrode driving circuits.

The closest arts, Motegi et al. as discussed above, either singularly or in combination, fails to anticipate or render obvious the above limitations obvious.

Response to Amendment

6. Applicant's arguments filed 8/16/2004 have been fully considered but they are persuasive for claims 1 to 4 and however, not persuasive for claims 5 to 8. The applicant argued that the prior art, Motegi et al. shows four column drivers 21 clearly connected in series but examiner again disagrees with the applicant because those column drivers are connected in series with each other (see fig.7). The applicant argued that the prior art, Motegi et al., does not show a timing signal that is supplied on the specific path defined by claims 5 to 8 and examiner disagrees with the applicant because it would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the timing signal which is inherently included in the controller 23

of Figure 7 in the column driver 21 closest to the row driver 23 in order to save space. The controller 23 may not show a timing signal but it is inherent in the controller. The applicant has to amend the claims to really claim the specific invention to overcome this prior art. Therefore the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 12/23/2004

HENRY N. TRAN
PRIMARY EXAMINER